



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/437,135	11/10/1999	SHUNPEI YAMAZAKI	0756-2064	7576

7590 03/12/2004

SIXBEY FRIEDMAN LEEDOM & FERGUSON PC
8180 GREENSBORO DRIVE SUITE 800
MCLEAN, VA 22102

EXAMINER

KIELIN, ERIK J

ART UNIT	PAPER NUMBER
----------	--------------

2813

DATE MAILED: 03/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/437,135	Applicant(s) YAMAZAKI ET AL. OK	
	Examiner Erik Kielin	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-37 is/are pending in the application.
- 4a) Of the above claim(s) 15-28 and 30-37 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 and 29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>1/8/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election of the Species of Group II, claims 1-14 and 29 in Paper filed 6 January 2004 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).
2. Claims 30-37 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
4. Claims 1, 4 and 6, 9 and 11, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,274,279 (**Misawa et al.**) in view of Applicant's admitted prior art (**APA**) and further in view of JP 63-4624 (**Hamazaki et al.**).

Regarding independent claims 1, 6, and 11, **Misawa** discloses a method of forming semiconductor devices, which are CMOS TFTs, comprising the steps of,

forming first, second, and third, patterned, crystallized col. 9, lines 19-26), silicon semiconductor islands **111**, **112**, **113** over a transparent substrate **110** (Figs. 4A; col. 7, lines 60-66);

forming gate insulating films **114, 115, 116** formed from silicon oxides (as further limited by instant claims 6 and 30; col. 6, lines 39-46) on each of the semiconductor islands using chemical vapor deposition (Fig. 4A; sentence bridging cols. 7-8);

forming gate electrodes **117, 118, 119** on each of the gate insulating films (Fig. 4A; sentence bridging cols. 7-8);

introducing phosphorous into said first and second semiconductor islands and introducing boron into said second semiconductor island, wherein a dose amount of said boron is larger than that of said phosphorous (col. 8, lines 3-56 -- **especially lines 50-56**).

Misawa is silent to the method by which the semiconductor islands are formed, but as noted above indicates that they are polycrystalline at col. 9, lines 19-26.

The **APA** discloses that it is known in the art to make a TFT by forming a semiconductor film comprising amorphous silicon over a substrate; crystallizing said semiconductor film by irradiating a laser light. (Applicant's specification, pages 2-4).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to apply the silicon islands **111, 112, 113** of **Misawa** by depositing amorphous silicon and laser crystallizing as taught by **APA**, because **Misawa** is silent to the method by which such polycrystalline patterned silicon islands are formed, such that one of ordinary skill would be motivated to use known methods for forming such as that taught by **APA** to be known specifically for TFTs such as **Misawa** is making. One of ordinary skill is motivated to save the time and money otherwise devoted to costly research and development by using, instead, known methods which are already proven to accomplish the desired objective, in this case, forming crystalline semiconductor islands for use as transistors.

Misawa does not teach that the gate insulating layers of silicon oxides **114, 115, 116**, disclosed therein as deposited by plasma CVD using TEOS and that the gate insulating layers are laser irradiated.

The **APA** also discloses that it is known to use plasma deposited TEOS as a gate insulator and that TEOS-deposited films require an oxidizing anneal (i.e. an anneal in an oxygen gas) to be used as gate insulating films. (See the instant specification section entitled, "Prior Art" -- especially the last two paragraphs.)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use plasma CVD using TEOS followed by oxidizing annealing, as taught by **APA**, as the method of depositing the gate insulation of **Misawa**, because **Misawa** is silent to which type of CVD deposition is used such that one of ordinary skill would be motivated to use known CVD methods and precursors to save time and money and research and development otherwise required to determine which CVD method and precursors to use.

Then the only difference is that **Misawa** and **APA** do not teach that the annealing of the gate insulating films is performed using a laser.

Hamazaki (the reference provided by Applicant) teaches the benefits of laser annealing a gate dielectric in an oxygen environment using a laser to reduce the surface states to less than 10^{11} cm^{-2} --as further limited by instant claims 4, 9, and 29. (See Hamazaki, Title, Abstract, and Fig. 2.)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use laser annealing in oxygen as the annealing method of **APA** because **APA** is silent to the

annealing heat source, and one of ordinary skill would be motivated to use laser annealing to reduce the surface states, as taught by **Hamazaki**.

Regarding claims 2, 7, and 12, the laser light of **Hamazaki** is inherently a "pulse laser light" by virtue of the fact that it can be turned on and off and one of ordinary skill would know that the pulse could run from the beginning to the end of the anneal cycle. Presently there exists no requirement that the laser light be pulsed during the anneal of the gate insulating film. In this regard, it has been held that to be entitled to weight in method claims, the recited structure limitations therein must affect the method in a manipulative sense, and not amount to the mere claiming of a use of a particular structure. *Ex parte Pfeiffer*, 1962, C.D. 408 (1961).

Regarding claims 3, 8, and 13, **Hamazaki** does not indicate the power of the laser. However, these claims are obvious in the absence of an unexpected result. One of ordinary skill would be motivated to optimize the laser power so as to achieve the result of reduced surface state density, as taught by **Hamazaki**, without also damaging the **Misawa** device. In this regard, it has been held, "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955). See also *In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmischer* 66 USPQ 314

Art Unit: 2813

(CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sold* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

5. Claims 5, 10, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Misawa** in view of the **APA** and **Hamazaki** as applied to claims 1, 6, and 11 above, and further in view of **JP 60-187030**.

Hamazaki does not indicate the kind of laser to be used for crystallizing the silicon film.

JP 60-187030 discloses the benefits of the instantly claimed excimer lasers for such crystallizing silicon which are inherently pulsed (Abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to crystallize the silicon using the lasers in **JP 60187030** for the reasons indicated therein and because excimer lasers are known for the purpose of crystallization of silicon films.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached on 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2813

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Erik Kielin
Primary Examiner
8 March 2004